ABSTARCT OF THE DISCLOSURE

There are provided a semiconductor memory device incorporating an ECC which enables an efficient test with high accuracy by a simplified structure and can shorten the test time and a test method thereof. A semiconductor memory device has an ECC circuit capable of correcting, from an m-bit information code and an n-bit check code stored in an information storing part, an error of the information code to x bits, and a parallel test circuit for receiving an information code and a check code for test with the same bits stored in the information storing part and deciding a defect with the x+1 bits or more as being defective. The parallel test circuit decides a defect with the x+1 bits or more for one piece of position information as a defective chip.